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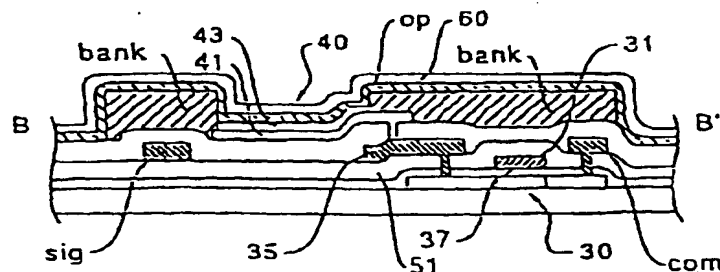
(54) **ACTIVE MATRIX DISPLAY**

(57) In an active matrix display device 1 in accordance with the present invention, each pixel 7 is provided with a pixel electrode 41, an organic semiconductor film 43 deposited on the upper layer side of the pixel electrode 41, and a thin film luminescent element 40 provided with an opposed electrode *op* formed on the upper layer side of the organic semiconductor film 43. A

protective film 60 covering almost the entire surface of a substrate is formed on the upper layer of the opposed electrode *op*. The protective film 60 prevents the entry of moisture or oxygen to inhibit the deterioration of the thin film luminescent element 40.

[FIG. 3]

(B)



## Description

### Field of the Invention

[0001] The present invention relates to an active matrix display device wherein the drive of a thin film luminescent element such as an electroluminescent element (hereinafter referred to as an "EL element") or a light emitting diode element (hereinafter referred to as an "LED element"), which emits light when drive current passes through a luminescent thin film such as an organic semiconductor film, is controlled by a thin film transistor (hereinafter referred to as a "TFT").

### Background Art

[0002] An active matrix display device has been proposed which employs a current-controlled luminescent element such as an EL element or an LED element. All these luminescent elements are self-luminescent, making them advantageous in that they do not need a back-light that is required in the case of a liquid crystal display device and that they depend less on viewing angles.

[0003] Figure 4 is a block diagram of an active matrix display device employing an EL element that emits light by means of a charge-injection type organic semiconductor thin film. Disposed on a transparent substrate 10 of an active matrix display device 1A are a plurality of scanning lines *gate*, a plurality of data lines *sig* extended in such a direction that they intersect with the direction in which the scanning lines *gate* are extended, a plurality of common feeder lines *com* parallel to the data lines *sig*, and pixels 7 formed in a matrix pattern by the data lines *sig* and the scanning lines *gate*. A data side drive circuit 3 and a scanning side drive circuit 4 are configured for the data lines *sig* and the scanning lines *gate*. Provided for each pixel 7 are a conduction control circuit 50 to which scanning signals are supplied via the scanning lines *gate*, and a thin film luminescent element 40 that emits light in accordance with image signals supplied through the data lines *sig* via the conduction control circuit 50. The conduction control circuit 50 is constituted by a first TFT 20 in which scanning signals are supplied to a gate electrode thereof via the scanning lines *gate*, a retention capacitor *cap* that retains image signals supplied through the data lines *sig* via the first TFT 20, and a second TFT 30 in which the image signals retained by the retention capacitor *cap* are supplied to a gate electrode thereof. The second TFT 30 and the thin film luminescent element 40 are connected in series between an opposed electrode *op* and the common feeder lines *com* to be discussed hereinafter. When the second TFT 30 is placed in an ON state, drive current passes through the common feeder lines *com*, causing the thin film luminescent element 40 to emit light, and the luminescent state is retained by the retention capacitor *cap* for a predetermined period of time.

[0004] Figure 5 is a top plan view showing one of the pixels included in the active matrix display device shown in Fig. 4. Figures 6(A), (B), and (C) are a sectional view taken at the line A-A', a sectional view taken at the line B-B', and a sectional view taken at the line C-C' of Fig. 5, respectively.

[0005] In the active matrix display device 1A having such a configuration, the first TFT 20 and the second TFT 30 are formed in the same process by utilizing island-like semiconductor films in every pixel 7 as shown in Fig. 5 and Fig. 6(A) and (B). The first TFT 20 has a gate electrode 21 configured as a part of the scanning line *gate*. In the first TFT 20, the data line *sig* is electrically connected via a contact hole of a first interlayer insulating film 51 to one end of a source and drain region, while a drain electrode 22 is electrically connected to the other end thereof. The drain electrode 22 is extended toward the region where the second TFT 30 is formed. A gate electrode 31 of the second TFT 30 is electrically connected to the extended portion via a contact hole of the first interlayer insulating film 51. A relay electrode 35 is electrically connected to one end of the source and drain region of the second TFT 30 via the contact hole of the first interlayer insulating film 51. A pixel electrode 41 of the thin film luminescent element 40 is electrically connected to the relay electrode 35 via a contact hole of a second interlayer insulating film 52.

[0006] As can be seen from Fig. 5 and Fig. 6(B) and (C), the pixel electrode 41 is formed independently for each pixel 7. On the upper layer side of the pixel electrode 41, an organic semiconductor film 43 and the opposed electrode *op* are laminated in this order. The opposed electrode *op* is formed so that it covers at least a display section 11.

[0007] Referring back to Fig. 5 and Fig. 6(A), the common feeder line *com* is electrically connected to the other end of the source and drain region of the second TFT 30 via the contact hole of the first interlayer insulating film 51. An extended portion 39 of the common feeder line *com* is opposed to an extended portion 36 of the gate electrode 31 of the second TFT 30, with the first interlayer insulating film 51 sandwiched therebetween as a dielectric film thereby to form the retention capacitor *cap*.

[0008] The active matrix display device 1A provides a great advantage in that the opposed electrode *op* deposited on the transparent substrate 10 obviates the need of laminating an opposed substrate, differentiating itself from an active matrix liquid crystal display device. However, the thin film luminescent element 40 is simply covered by the thin opposed electrode *op*, so that moisture or oxygen intrudes into the organic semiconductor film 43 by diffusing and transmitting through the opposed electrode *op*, leading to a danger of deteriorated luminous efficiency, a higher drive voltage (shift of a threshold voltage to a higher voltage side), and deteriorated reliability of the thin film luminescent element

40. To prevent the entry of the moisture or oxygen, the conventional active matrix display device 1A has been employing a method wherein at least the display section 11 is covered by an opposed substrate, and the outer periphery of the opposed substrate has been sealed. This method, however, inevitably sacrifices the advantage over the liquid crystal display device.

[0009] Accordingly, an object of the present invention is to provide an active matrix display device capable of protecting a thin film luminescent element from moisture, etc. by means of a simple structure.

#### Disclosure of the Invention

[0010] The active matrix display device in accordance with the present invention has the following configuration.

[0011] The active matrix display device has a display section on a substrate, the display section being formed by a plurality of scanning lines, a plurality of data lines intersecting with the scanning lines, and a plurality of pixels formed in a matrix pattern by the data lines and the scanning lines, each of the pixels having a conduction control circuit including a thin film transistor to which a scanning signal is supplied to a gate electrode thereof via the scanning lines, a pixel electrode formed for each pixel, a luminescent thin film deposited on the upper layer side of the pixel electrode, and a thin film luminescent element equipped with an opposed electrode which is formed at least on the entire surface of the display section on the upper layer side of the luminescent thin film, and the thin film luminescent element emitting light in accordance with image signals supplied from the data lines via the conduction control circuit, wherein: a protective film, which covers at least a region where the opposed electrode is formed, is formed on the upper layer side of the opposed electrode.

[0012] According to the configuration, the thin film luminescent element can be protected against moisture, etc. that is diffused or transmitted through the opposed electrode since the protective film is formed on the upper layer side of the opposed electrode of the thin film luminescent element. Hence, it is possible to prevent deteriorated luminous efficiency, a rise in the drive voltage (the shift of a threshold voltage to the higher voltage side), deteriorated reliability, etc. in the thin film luminescent element. Moreover, the protective film can be easily formed by using a semiconductor process, so that it does not add to the manufacturing cost of the active matrix display device. Thus, the reliability of the active matrix display device can be improved, while retaining the advantage of the active matrix display device employing the thin film luminescent element in which no opposed substrate is required to be deposited. Furthermore, since the protective film protects the thin film luminescent element, the material used for the opposed electrode may be selected from the viewpoint mainly of the luminous efficiency or the drive voltage of

the thin film luminescent element, thus providing another advantage in that the material is not limited to one having high performance to protect the thin film luminescent element.

[0013] In the present invention, it is preferable that the luminescent thin film is partitioned by an insulating film formed on the lower layer side of the opposed electrode so that it is thicker than the organic semiconductor film. In the active matrix display device employing the thin film luminescent element, the opposed electrode is formed at least over the entire surface of the display section and opposed to the data line; therefore, a large parasitic capacitor is produced on the data line as it is. According to the present invention, however, the presence of the thick insulating film between the data line and the opposed electrode makes it possible to inhibit the parasitic capacitor from being produced on the data line. As a result, the load on a data side drive circuit can be reduced, enabling reduced power consumption or quicker display operation. In addition, the insulating film formed as mentioned above can be used as a bank layer for preventing a discharge liquid from spilling out when forming a luminescent thin film by the ink-jet process in a region partitioned by the insulating film.

[0014] In the present invention, preferably, the opposed electrode is formed of, for example, an aluminum film containing an alkali metal. When the opposed electrode is formed of such a film, the possibility of moisture, etc. being diffused or transmitted is higher; hence, the effect of the formation of the protective film is remarkable.

[0015] In the present invention, the protective film may be formed of an insulating film such as a silicon nitride film, or it may be formed of a conductive film of a metal having a high melting point or an alloy thereof. Further alternatively, the protective film may be formed of a conductive film such as a pure aluminum film, an aluminum film containing silicon, or an aluminum film containing copper. Further, the protective film may be formed of two layers consisting of a conductive film and an insulating film. When the protective film deposited on the opposed electrode is formed of a conductive film, the same effect that can be obtained from lowering the electrical resistance of the opposed electrode can be achieved. When the thick insulating film partitioning the region, where the organic semiconductor film is formed, is formed, the large difference in level produced by the insulating film may cause disconnection of the opposed electrode formed on the upper layer side thereof. Forming the protective film deposited on the opposed electrode of a conductive film makes it possible to prevent the disconnection of the opposed electrode because the conductive film forms a redundant wiring structure. Accordingly, even when the thick insulating film is formed around the organic semiconductor film to suppress a parasitic capacitance in an active matrix display device, the disconnection of the opposed electrode formed on the upper layer of the insulating film does not

occur, enabling improved display quality and reliability of the active matrix display device to be achieved.

[0016] In the present invention, the conduction control circuit is preferably provided with the first TFT wherein the scanning signals are supplied to the gate electrode thereof, and the second TFT wherein the gate electrode thereof is connected to the data lines via the first TFT, and the second TFT and the thin film luminescent element are connected in series between the common feeder line for supplying drive current, which is configured separately from the data lines and the scanning lines, and the opposed electrode. In other words, the conduction control circuit could be constructed by one TFT and a retention capacitor; however, it is preferable to configure the conduction control circuit of each pixel by two TFTs and a retention capacitor to accomplish higher display quality.

#### Brief Description of the Drawings

##### [0017]

Fig. 1 is a block diagram schematically showing an entire layout of an active matrix display device to which the present invention has been applied.

Fig. 2 is a top plan view of one of the pixels included in the active matrix display device shown in Fig. 1.

Fig. 3 (A), (B), and (C) are a sectional view taken at the line A-A', a sectional view taken at the line B-B', and a sectional view taken at the line C-C', respectively, of Fig. 2.

Fig. 4 is a block diagram schematically showing the entire layout of a conventional active matrix display device.

Fig. 5 is a top plan view of one of the pixels included in the active matrix display device shown in Fig. 4.

Fig. 6 (A), (B), and (C) are a sectional view taken at the line A-A', a sectional view taken at the line B-B', and a sectional view taken at the line C-C', respectively, of Fig. 5.

#### Description of Reference Numerals

##### [0018]

|    |                              |
|----|------------------------------|
| 1  | Active matrix display device |
| 2  | Display section              |
| 3  | Data side drive circuit      |
| 4  | Scanning side drive circuit  |
| 7  | Pixel                        |
| 10 | Transparent substrate        |
| 12 | Terminal                     |
| 20 | First TFT                    |
| 21 | Gate electrode of first TFT  |
| 30 | Second TFT                   |
| 31 | Gate electrode of second TFT |
| 40 | Luminescent element          |
| 41 | Pixel electrode              |

|       |                              |
|-------|------------------------------|
| 43    | Organic semiconductor        |
| 60    | Protective film              |
| bank  | Bank layer (Insulating film) |
| cap   | Retention capacitor          |
| 5 com | Common feeder line           |
| gate  | Scanning line                |
| op    | Opposed electrode            |
| sig   | Data line                    |

##### 10 Best Mode for Carrying Out the Invention

[0019] An embodiment of the present invention will be described with reference to the accompanying drawings. In the following description, the same reference numerals will be assigned to the components common to the elements described with reference to Fig. 4 to Fig. 6.

##### (Entire Configuration)

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[0020] Figure 1 is a block diagram schematically showing the entire layout of an active matrix display device; Fig. 2 is a top plan view of one of the pixels included therein; and Fig. 3 (A), (B), and (C) are a sectional view taken at the line A-A', a sectional view taken at the line B-B', and a sectional view taken at the line C-C', respectively, of Fig. 2.

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[0021] In an active matrix display device 1 shown in Fig. 1, the central portion of a transparent substrate 10, which is the base of the apparatus, provides a display section 11. In the outer peripheral portion of the transparent substrate 10, a data side drive circuit 3 that outputs image signals is formed at the ends of data lines *sig*, and a scanning side drive circuit 4 that outputs scanning signals is formed at the ends of scanning lines *gate*. In these drive circuits 3 and 4, complementary TFTs are formed by N-type TFTs and P-type TFTs, the complementary TFTs constituting a shift register circuit, a level shifter circuit, an analog switching circuit, etc. As in the active matrix substrate of an active matrix liquid crystal display device, the display section 11 has, on the transparent substrate 10, a plurality of pixels 7 formed in a matrix pattern by a plurality of scanning lines *gate* and a plurality of data lines *sig* extendedly provided in the direction to intersect with the direction in which the scanning lines *gate* are extendedly provided.

[0022] Each of the pixels 7 includes a conduction control circuit 50 to which scanning signals are supplied via the scanning lines *gate*, and a thin film luminescent element 40 that emits light in accordance with image signals supplied from the data lines *sig* via the conduction control circuit 50. The example shown herein is formed by a first TFT 20 wherein scanning signals are supplied to the gate electrode thereof via the scanning lines *gate*, a retention capacitor *cap* that retains image signals supplied from the data lines *sig* via the first TFT 20, and a second TFT 30 in which the image signals retained by the retention capacitor *cap* are supplied to

the gate electrode thereof. The second TFT 30 and the thin film luminescent element 40 are connected in series between an opposed electrode *op* and the common feeder lines *com* to be discussed in detail hereinafter.

[0023] In the active matrix display device 1 having such a configuration, the first TFT 20 and the second TFT 30 are formed by utilizing island-like semiconductor films (silicon films) in every pixel 7 as shown in Fig. 2 and Fig. 3(A) and (B).

[0024] The first TFT 20 has a gate electrode 21 configured as a part of the scanning line *gate*. In the first TFT 20, the data line *sig* is electrically connected via a contact hole of a first interlayer insulating film 51 to one end of a source and drain region, while a drain electrode 22 is electrically connected to the other end thereof. The drain electrode 22 is extendedly provided toward the region where the second TFT 30 is formed. A gate electrode 31 of the second TFT 30 is electrically connected to the extendedly provided portion via a contact hole of the first interlayer insulating film 51.

[0025] A relay electrode 35 that is formed at the same time as the data lines *sig* is electrically connected to one end of the source and drain region of the second TFT 30 via the contact hole of the first interlayer insulating film 51. A transparent pixel electrode 41 formed of an ITO film of the thin film luminescent element 40 is electrically connected to the relay electrode 35 via a contact hole of a second interlayer insulating film 52.

[0026] As can be seen from Fig. 2 and Fig. 3(B) and (C), the pixel electrode 41 is formed independently for each pixel 7. On the upper layer side of the pixel electrode 41, an organic semiconductor film 43 formed of polyphenylene vinylene (PPV) or the like and the opposed electrode *op* formed of a metal film composed of aluminum and calcium containing an alkali metal such as lithium are laminated in this order to constitute the thin film luminescent element 40. The organic semiconductor film 43 is formed for each pixel 7; however, it may be formed in stripes over a plurality of pixels 7 in some cases. The opposed electrodes *op* are formed over the entire display section 11 and the region except at least the peripheral area of the portion wherein terminals 12 are formed.

[0027] The thin film luminescent element 40 may have a structure that enhances the luminous efficiency (hole injection efficiency) by providing a hole injection layer, a structure that enhances the luminous efficiency (electron injection efficiency) by providing an electron injection layer, or a structure wherein both the hole injection layer and the electron injection layer are formed.

[0028] Referring back to Fig. 2 and Fig. 3(A), the common feeder line *com* is electrically connected to the other end of the source and drain region of the second TFT 30 via the contact hole of the first interlayer insulating film 51. An extendedly provided portion 39 of the common feeder line *com* is opposed to an extendedly provided portion 36 of the gate electrode 31 of the sec-

ond TFT 30, with the first interlayer insulating film 51 sandwiched therebetween as a dielectric film thereby to form the retention capacitor *cap*.

[0029] In the active matrix display device 1 configured as discussed above, when the first TFT 20 is selected by a scanning signal and placed in an ON state, the image signal from the data line *sig* is applied to the gate electrode 31 of the second TFT 30 via the first TFT 20, and the image signal is written to the retention capacitor *cap* via the first TFT 20. As a result, when the second TFT 30 is placed in the ON state, a voltage is applied, with the opposed electrode *op* and the pixel electrode 41 serving as the negative pole and the positive pole, respectively. In an area where the applied voltage exceeds a threshold voltage, the current (drive current) passing through the organic semiconductor film 43 suddenly increases. Hence, the luminescent element 40 emits light as an electroluminescent element or an LED element, and the light from the luminescent element 40 is reflected by the opposed electrode *op* and transmitted through the transparent pixel electrode 41 and the transparent substrate 10 before it goes out. The drive current for emitting the light goes through a current path constructed by the opposed electrode *op*, the organic semiconductor film 43, the pixel electrode 41, the second TFT 30, and the common feeder lines *com*. Therefore, when the second TFT 30 is placed in an OFF state, the current no longer passes. However, even when the first TFT 20 is placed in the OFF state, the gate electrode of the second TFT 30 is retained at a potential equivalent to the image signal by the retention capacitor *cap*, thus holding the second TFT 30 in the ON state. Accordingly, the drive current continues to pass through the luminescent element 40, and the pixel is held ON. This state is maintained until new image data is written to the retention capacitor *cap* and the second TFT 30 is placed in the OFF state.

(Protective Structure of Thin Film Luminescent Element)

[0030] Thus, the active matrix display device 1 employing the thin film luminescent element 40 provides a great advantage in that the opposed electrode *op* deposited on the transparent substrate 10 itself obviates the need of laminating an opposed substrate, differentiating itself from an active matrix liquid crystal display device. However, there is a danger in that moisture or oxygen intrudes into the thin film luminescent element 40 by diffusion and transmission through the thin opposed electrode *op*. Particularly in this embodiment, an aluminum film containing an alkali metal such as lithium is employed for the opposed electrode *op* in order to enhance the electron injection efficiency in the thin film luminescent element 40 so as to lower the drive voltage, whereas the aluminum film containing an alkali metal is considered to permit diffusion and transmission of moisture or oxygen more easily than pure aluminum

does. More specifically, the aluminum film containing an alkali metal exhibits lower toughness than a pure aluminum film, an aluminum film containing silicon, or an aluminum film containing copper, so that it is apt to break when subjected to stress, leading to a possibility of the entry of moisture or oxygen through a crack or the like. Further, a fracture surface of an aluminum film containing an alkali metal shows a columnar texture, and it is conceivable that moisture or oxygen is easily diffused and transmitted through the texture.

[0031] For the reason described above, a protective film 60 composed of pure aluminum is formed on the upper layer of the opposed electrode *op*. The protective film 60 formed of pure aluminum has toughness that is sufficiently high to survive stress to a certain extent, so that it inhibits the occurrence of a crack that leads to a path for the entry of moisture or oxygen. Further, the fracture surface of pure aluminum does not exhibit a columnar texture observed in the aluminum film containing an alkali metal, eliminating the possibility of entry of moisture or oxygen through the texture. Hence, the active matrix display device 1 of this embodiment is capable of protecting the thin film luminescent element 40 from moisture, etc., thus inhibiting deterioration in the luminous efficiency, an increase in the drive voltage (the shift of the threshold voltage to the higher voltage side), deterioration in reliability, etc. of the thin film luminescent element 40. Moreover, the protective film 60 formed of the pure aluminum film can be easily formed by utilizing a semiconductor process; therefore, it does not add to the manufacturing cost of the active matrix display device 1. This makes it possible to improve the reliability of the active matrix display device 1 while retaining the advantage of the active matrix display device 1 employing the thin film luminescent element 40 in which there is no need to deposit an opposed substrate.

[0032] In addition, since the protective film 60 protects the thin film luminescent element 40, the material used for the opposed electrode *op* may be selected from the viewpoint mainly of the luminous efficiency or the drive voltage of the thin film luminescent element 40, thus providing another advantage in that the material is not limited to one having high performance to protect the thin film luminescent element 40.

[0033] Furthermore, in this embodiment, the protective film 60 deposited on the opposed electrode *op* is formed of a conductive film composed of the pure aluminum film, so that the same advantage obtained by lowering the electrical resistance of the opposed electrode *op* can be achieved.

#### (Structure of Bank Layer)

[0034] In the active matrix display device 1 configured as described above, in order to protect the data lines *sig* from a large parasitic capacitor, the embodiment is provided with a thick insulating film (a bank layer *bank*/the

hatched area) formed of a resist film or a polyimide film along the data lines *sig* and the scanning lines *gate* as shown in Fig. 1, Fig. 2, and Fig. 3 (A), (B), and (C), and the opposed electrode *op* is formed on the upper layer side of the bank layer *bank*. Hence, the presence of a second interlayer insulating film 52 and the thick bank layer *bank* between the data lines *sig* and the opposed electrode *op* controls the capacitance parasitic to the data lines *sig* to an extremely small value. This makes it possible to reduce the load on the drive circuits 3 and 4 and to achieve reduced power consumption and quicker display operation.

[0035] Further, as shown in Fig. 1, the bank layer *bank* (the formation area is hatched) is formed also in a peripheral area of the transparent substrate 10 (area outside the display section 11). Accordingly, both the data side drive circuit 3 and the scanning side drive circuit 4 are covered by the bank layer *bank*. The opposed electrode *op* is formed in at least in the display section 11, and it is not required to be formed in the area wherein the drive circuits are formed. However, the opposed electrode *op* is normally formed by mask sputtering, and poor alignment accuracy causes the opposed electrode *op* to be superimposed on the drive circuits in some cases. Even if the opposed electrode *op* should overlap the area wherein the drive circuits are formed as mentioned above, the presence of the bank layer *bank* between the wiring layers of the drive circuits and the opposed electrode *op* prevents the capacitor from being parasitic to the drive circuits 3 and 4. This makes it possible to reduce the load on the drive circuits 3 and 4 and to achieve reduced power consumption and quicker display operation.

[0036] Further in this embodiment, the bank layer *bank* is also formed in an area of the region where the pixel electrode 41 is formed, the area overlapping the relay electrode 35 of the conduction control circuit 50. Therefore, the organic semiconductor film 43 is not formed in the area overlapping the relay electrode 35. This means that the organic semiconductor film 43 is formed only in a flat area of the region where the pixel electrode 41 is formed, so that the organic semiconductor film 43 is produced to have a constant thickness, thus preventing nonuniform display. The absence of the bank layer *bank* in the area overlapping the relay electrode 35 causes the drive current to be passed between the relay electrode 35 and the opposed electrode *op* in the area, and the organic semiconductor film 43 emits light. The light, however, does not exit the device because it is held between the relay electrode 35 and the opposed electrode *op* and therefore does not contribute to display. The drive current passed through the area that does not contribute to display may be considered as invalid current from the viewpoint of display. In this embodiment, however, the bank layer *bank* is formed in the area, wherein such an invalid current used to be passed through, so as to prevent the drive current from being passed therethrough. This makes it possible

to prevent wasteful current from being passed through the common feeder lines *com*; hence, the width of the common feeder lines *com* can be made smaller accordingly. As a result, the luminescent area can be increased, enabling improved display performance including luminance and contrast ratio to be achieved.

[0037] When the thick bank layer *bank* is formed, there is a danger in that a large step *bb* formed by the bank layer *bank* shown in Fig. 3 causes the disconnection of the opposed electrode *op* formed on the upper layer side. In this embodiment, however, the protective film 60 deposited on the opposed electrode *op* is formed of a conductive film, and a redundant wiring structure is configured by the conductive film (the protective film 60). Therefore, even when the thick bank layer *bank* is formed to suppress a parasitic capacitor or the like, the opposed electrode *op* formed on the upper layer of the bank layer *bank* will not incur disconnection, thus permitting improved display quality and reliability of the active matrix display device 1.

[0038] If the bank layer *bank* is formed using a black resist, then the bank layer *bank* functions as a black matrix, which improves display quality including contrast ratio. In other words, in the active matrix display device 1 according to the embodiment, the opposed electrode *op* is formed on the entire surface of the pixel 7 on the surface side of the transparent substrate 10, and the light reflected by the opposed electrode *op* deteriorates the contrast ratio. Using the black resist for the bank layer *bank*, which serves to prevent the parasitic capacitor, causes the bank layer *bank* to function as the black matrix and blocks the light reflected from the opposed electrode *op*, thus leading to a higher contrast ratio.

(Manufacturing Method of Active Matrix Display device)

[0039] The bank layer *bank* formed as described above surrounds the region wherein the organic semiconductor film 43 is formed; therefore, it dams up a discharge liquid to prevent it from protruding sideways when the organic semiconductor film 43 is produced using a liquid material discharged from an ink-jet head (a discharged liquid) in the manufacturing process of the active matrix display device. In the manufacturing method of the active matrix display device 1 to be described below, the steps for forming the first TFT 20 and the second TFT 30 on the transparent substrate 10 are nearly the same as those for manufacturing an active matrix substrate of the liquid crystal active matrix display device 1. Hence, the outline of the process will be briefly explained with reference to Fig. 3 (A), (B), and (C).

[0040] First, a foundation protective film (not shown) composed of a silicon oxide film that is about 2000 to about 5000 angstroms thick is formed on the transparent substrate 10 by the plasma CVD technique using TEOS (tetraethylorthosilicate) or oxygen gas as the material gas as necessary. Then, a semiconductor film

composed of an amorphous silicon film having a thickness of about 300 to about 700 angstroms is formed on the surface of the foundation protective film by the plasma CVD technique. Subsequently, the semiconductor film formed of the amorphous silicon film is subjected to a crystallizing process such as laser annealing or solid phase growth technique to crystallize the semiconductor film into a polysilicon film.

[0041] Next, the semiconductor film is patterned to form it into an island-like semiconductor film, and a gate insulating film 37 composed of a silicon oxide film or nitride film having a thickness of about 600 to about 1500 angstroms is formed on the surface of the island-like semiconductor film by the plasma CVD technique using TEOS (tetraethylorthosilicate) or oxygen gas as the material gas.

[0042] Subsequently, a conductive film that is formed of a metal film composed of aluminum, tantalum, molybdenum, titanium, or tungsten is formed by the sputtering technique, then patterning is carried out to form gate electrodes 21 and 31, and the extendedly provided portion 36 of the gate electrode 31 (a gate electrode forming step). In this step, the scanning lines *gate* are also formed.

[0043] In this state, high concentration phosphorus ions are implanted to produce the source and drain regions in a self-alignment fashion with respect to the gate electrodes 21 and 31. A portion where no impurity has been introduced provides a channel region.

[0044] Next, after the first interlayer insulating film 51 is formed, the respective contact holes are formed, and the data line *sig*, the drain electrode 22, the common feeder line *com*, the extendedly provided portion 39 of the common feeder line *com*, and the relay electrode 35 are formed. As a result, the first TFT 20, the second TFT 30, and the retention capacitor *cap* are formed.

[0045] Then, the second interlayer insulating film 52 is formed, and a contact hole is formed in a portion of the interlayer insulating film that corresponds to the relay electrode 35. After an ITO film is formed on the entire surface of the second interlayer insulating film 52, patterning is carried out to form the pixel electrode 41 for each pixel 7, the pixel electrode 41 being electrically connected to the source and drain regions of the second TFT 30 via the contact hole.

[0046] In the following step, a resist layer is formed on the surface of the second interlayer insulating film 52, then it is patterned so that the resist is left along the scanning line *gate* and the data line *sig* to form the bank layer *bank*. At this time, the resist portion to be left along the data line *sig* should be wide enough to cover the common feeder line *com*. As a result, the region wherein the organic semiconductor film 43 of the luminescent element 40 is to be deposited is surrounded by the bank layer *bank*. Then, the organic semiconductor films 43 corresponding to R, G, and B, respectively, are formed in the region defined in a matrix pattern by the bank layer *bank* by using the ink-jet process. For this

purpose, a liquid material (precursor) for making the organic semiconductor film 43 is discharged from an ink-jet head to the region inside the bank layer *bank*, and the discharged liquid material is fixed in the region inside the bank layer *bank* to form the organic semiconductor film 43. The bank layer *bank* is formed of a resist, so that it is water-repellent, whereas the precursor of the organic semiconductor film 43 employs a hydrophilic solvent. Hence, the applied region of the organic semiconductor film 43 is securely partitioned by the bank layer *bank* and does not protrude to the adjacent pixel 7. This enables the organic semiconductor film 43 to be formed only in a predetermined region. In this step, the precursor discharged from the ink-jet head expands to have a thickness of about 2  $\mu\text{m}$  to about 4  $\mu\text{m}$  due to surface tension; therefore, the bank layer *bank* is required to have a thickness of about 1  $\mu\text{m}$  to about 3  $\mu\text{m}$ . The thickness of the organic semiconductor film 43 after it has been fixed ranges from about 0.05  $\mu\text{m}$  to about 0.2  $\mu\text{m}$ . If the partition formed of the bank layer *bank* has a height of 1  $\mu\text{m}$  or more from the beginning, then the bank layer *bank* will satisfactorily function as the partition even if the bank layer *bank* is not water repellent. Forming the thick bank layer *bank* beforehand makes it possible to define the region wherein the organic semiconductor film 43 is to be formed when forming the organic semiconductor film 43 by applying another process in place of the ink-jet process.

[0047] After that, the opposed electrode *op* is formed on nearly the entire surface of the transparent substrate 10, and the protective film 60 is deposited on the upper layer of the opposed electrode *op*. The protective film 60 will securely provide sufficient resistance to humidity if it has a thickness of about 2000 angstroms to about 1  $\mu\text{m}$ .

[0048] According to the manufacturing method, the respective organic semiconductor films 43 corresponding to R, G, and B can be formed in predetermined regions by using the ink-jet process, permitting the manufacture of the active matrix display device 1 of a full-color feature with higher productivity.

[0049] The TFTs are formed also in the data side drive circuit 3 and the scanning side drive circuit 4 shown in Fig. 1. These TFTs are formed using all or some of the steps for forming the TFTs in the pixels 7. This means that the TFTs constituting the drive circuits are formed between the same layers as the TFTs of the pixels 7. Regarding the first TFT 20 and the second TFT 30, both may be of the N-type or P-type, or one of them may be the N-type while the other may be the P-type. Regardless of the combinations of the N-type and the P-type, the TFTs can be formed by a well-known process; therefore, the description thereof will be omitted.

[Other Embodiments]

[0050] The protective film 60 may be produced in the same manner as that in the embodiment described

above by using other metal films formed of an aluminum film containing silicon or an aluminum film containing copper or other metal besides the pure aluminum film as long as it is a conductive film that transmits less moisture or oxygen. Further, the protective film 60 may employ a metal having a high melting point or an alloy or the like thereof. Furthermore, using an insulating film such as a silicon nitride film as the protective film 60 permits the inhibition of deterioration in the thin film luminescent element 40. In addition, the protective film 60 may be of a double-layer structure consisting of an insulating film and a conductive film. In this case, depositing the conductive film on the opposed electrode *op* permits the implementation of the foregoing redundant wiring structure. In any case, the protective film is able to secure satisfactory resistance to humidity as long as it has a thickness of about 2000 angstroms to about 1  $\mu\text{m}$ .

[0051] When a resist film or a polyimide film formed of an organic material is used for the bank layer *bank* (insulating film), a thick film can be easily formed. When the bank layer *bank* (insulating film) is formed of a silicon oxide film or a silicon nitride film made of an inorganic material and formed by using the CVD process or the SOG process, the deterioration of the organic semiconductor film 43 can be inhibited even if the bank layer *bank* is in contact with the organic semiconductor film 43.

[0052] Further, besides the configuration in which the retention capacitor *cap* is formed in relation to the common feeder line *com*, the retention capacitor *cap* may be configured so that it is formed in relation to a capacitive line provided in parallel to the scanning line *gate*, or it may be configured by using the drain region of the first TFT 20 and the gate electrode 31 of the second TFT 30.

[0053] As described above, the active matrix display device has a protective film formed on the upper layer side of an opposed electrode of a thin film luminescent element, enabling the thin film luminescent element to be protected against moisture, etc. Hence, there is not a possibility of deterioration of the thin film luminescent element. Moreover, the protective film can be easily formed by utilizing a semiconductor process, so that it does not add to the manufacturing cost of the active matrix display device. Therefore, the reliability of the active matrix display device can be improved, while retaining the advantage of the active matrix display device employing the thin film luminescent element in which no opposed substrate is required to be deposited. Furthermore, since the protective film protects the thin film luminescent element, the material used for the opposed electrode may be selected from the viewpoint mainly of the luminous efficiency or the drive voltage of the thin film luminescent element, thus providing another advantage in that the material is not limited to one having high performance to protect the thin film luminescent element.



## Industrial Applicability

[0054] Having the advantages described above, the present invention is ideally used as an active matrix display device in which the drive of a thin film luminescent element such as an electroluminescent element or a light emitting diode element is controlled by thin film transistors. Furthermore, an active matrix display device to which the present invention has been applied can be extensively used not only for a personal computer, a portable information terminal but also for information display equipment including an outdoor large bulletin board and an advertisement signboard.

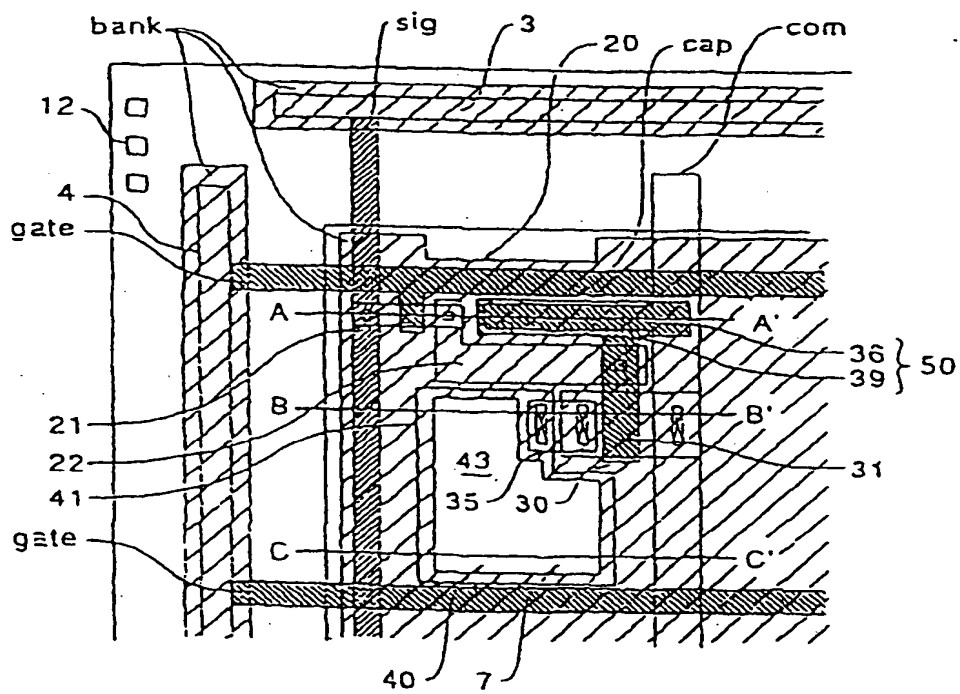
## Claims

1. An active matrix display device comprising a display section on a substrate, the display section being formed by a plurality of scanning lines, a plurality of data lines intersecting with the scanning lines, and a plurality of pixels formed in a matrix pattern by the data lines and the scanning lines, each of the pixels having a conduction control circuit including a thin film transistor to which a scanning signal is supplied to a gate electrode thereof via the scanning lines, a pixel electrode formed for each pixel, a luminescent thin film deposited on the upper layer side of the pixel electrode, and a thin film luminescent element equipped with an opposed electrode which is formed at least on the entire surface of the display section on the upper layer side of the luminescent thin film, and the thin film luminescent element emitting light in accordance with image signals supplied from the data lines via the conduction control circuit, wherein:
 

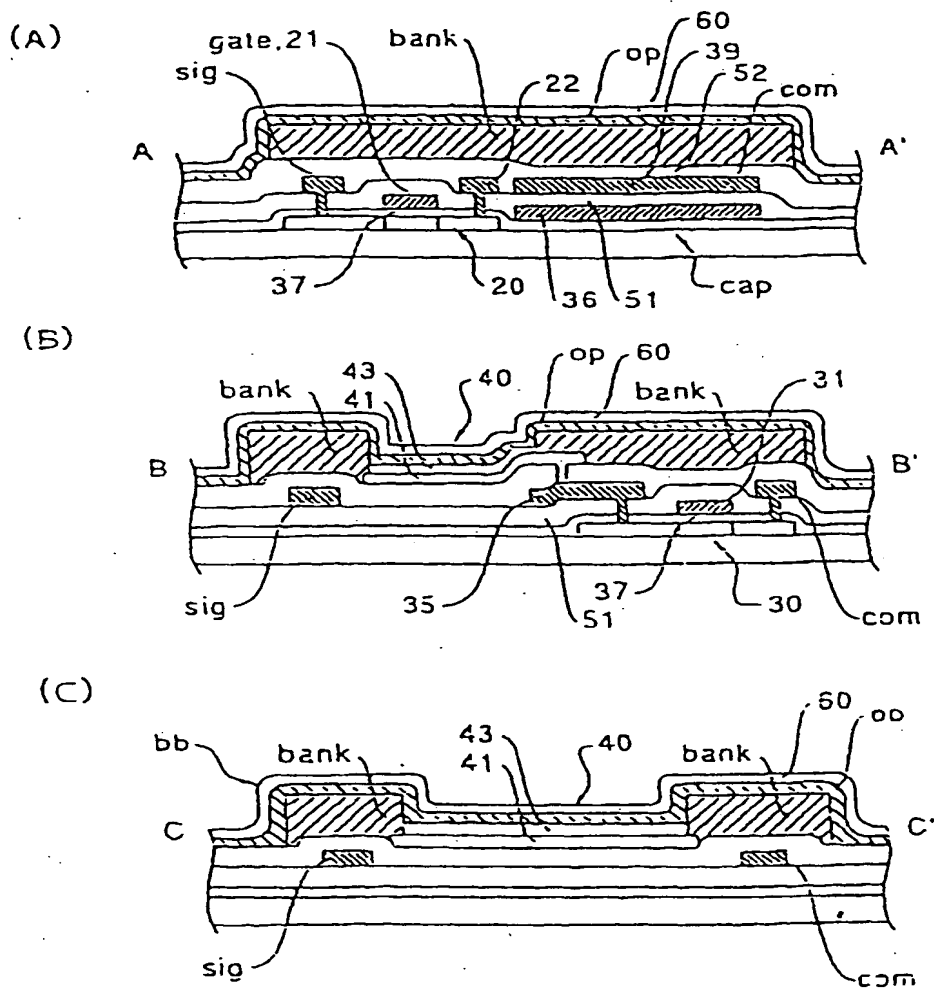
a protective film, which covers at least a region where the opposed electrode is formed, is formed on the upper layer side of the opposed electrode.
2. An active matrix display device according to Claim 1, wherein the luminescent thin film is partitioned by an insulating film that is formed on the lower layer side of the opposed electrode and formed to be thicker than the luminescent thin film.
3. An active matrix display device according to Claim 1 or 2, wherein the opposed electrode is formed of an aluminum film containing an alkali metal.
4. An active matrix display device according to Claim 1 or 2, wherein the protective film is formed of an insulating film.
5. An active matrix display device according to Claim 3, wherein the protective film is formed of an insulating film.
6. An active matrix display device according to Claim 1 or 2, wherein the protective film is formed of a silicon nitride film.
7. An active matrix display device according to Claim 3, wherein the protective film is formed of a silicon nitride film.
8. An active matrix display device according to Claim 1 or 2, wherein the protective film is formed of a metal having a high melting point or an alloy thereof.
9. An active matrix display device according to Claim 3, wherein the protective film is formed of a metal having a high melting point or an alloy thereof.
10. An active matrix display device according to Claim 1 or 2, wherein the protective film is formed of an aluminum film of any of a pure aluminum film, an aluminum film containing silicon, and an aluminum film containing copper.
11. An active matrix display device according to Claim 3, wherein the protective film is formed of an aluminum film of any of a pure aluminum film, an aluminum film containing silicon, and an aluminum film containing copper.
12. An active matrix display device according to Claim 1 or 2, wherein the protective film has a double-layer structure consisting of a conductive film and an insulating film.
13. An active matrix display device according to Claim 3, wherein the protective film has a double-layer structure consisting of a conductive film and an insulating film.
14. An active matrix display device according to Claim 1, wherein: the conduction control circuit comprises a first thin film transistor in which the scanning signal is supplied to a gate electrode thereof and a second thin film transistor having a gate electrode thereof connected to the data line via the first thin film transistor; and the second thin film transistor and the thin film luminescent element are connected in series between a common feeder line for supplying drive current that is configured separately from the data line and the scanning line, and the opposed electrode.



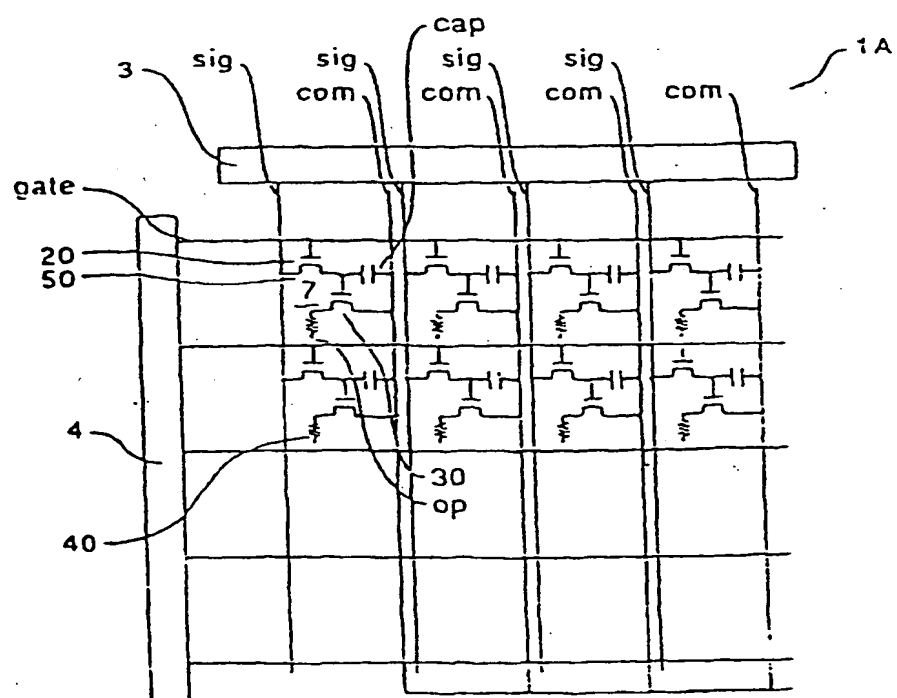
[FIG. 2]



[FIG. 3]

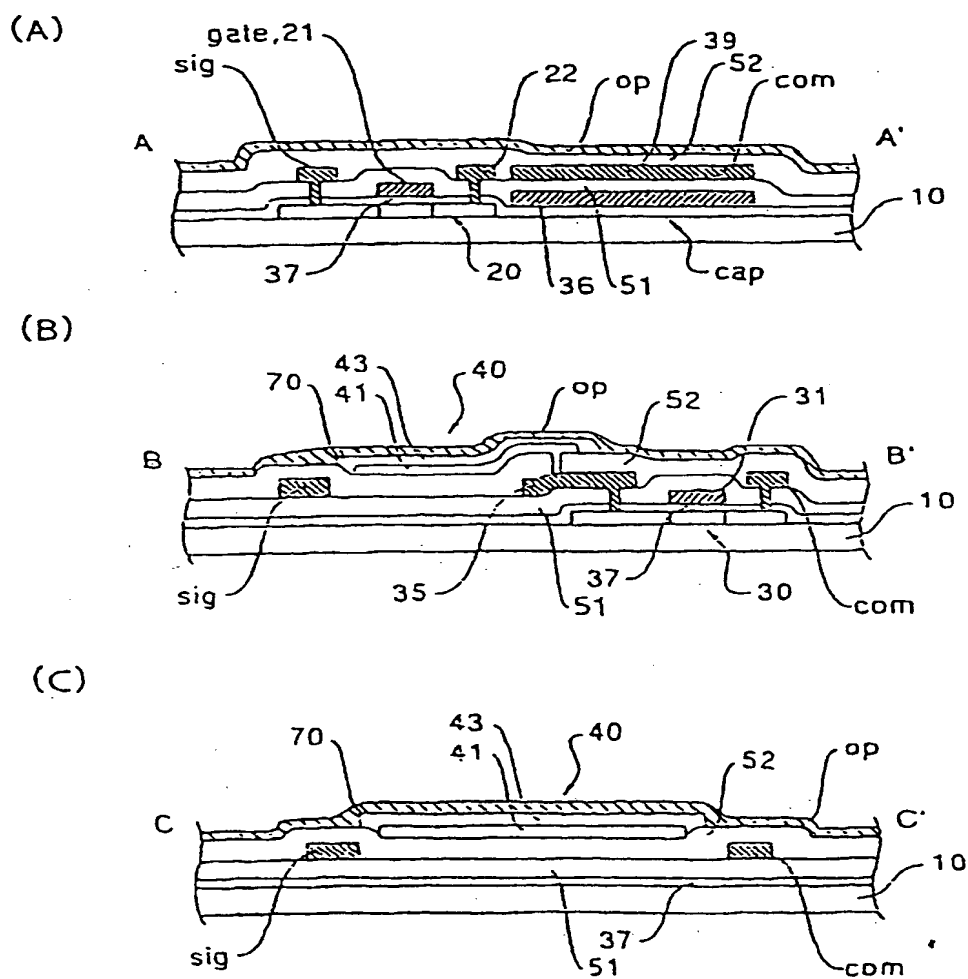


[FIG. 4]





[FIG. 6]



## INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP98/03758

| <b>A. CLASSIFICATION OF SUBJECT MATTER</b><br>Int.Cl. <sup>6</sup> H05B33/04, H05B33/22, H05B33/26, G02F1/136<br>According to International Patent Classification (IPC) or to both national classification and IPC   |   |  |
|--|---|--|
| <b>B. FIELDS SEARCHED</b><br>Minimum documentation searched (classification system followed by classification symbols)<br>Int.Cl. <sup>6</sup> H05B33/00-33/28<br>Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched<br>Jitsuyo Shinan Koho 1940-1996 Toroku Jitsuyo Shinan Koho 1994-1998<br>Kokai Jitsuyo Shinan Koho 1971-1998 Jitsuyo Shinan Toroku Koho 1996-1998<br>Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)  |   |  |
| <b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>  |   |  |
| Category*  | Citation of document, with indication, where appropriate, of the relevant passages                                      | Relevant to claim No.  |
| X  | JP, 8-227276, A (Pioneer Electronic Corp.),<br>3 September, 1996 (03. 09. 96),<br>Full text ; Figs. 1 to 14             | 1, 2, 14   |
| Y  | Full text ; Figs. 1 to 14 (Family: none)  | 3-13   |
| Y  | JP, 7-312290, A (NEC Corp.),<br>28 November, 1995 (28. 11. 95),<br>Full text ; Figs. 1 to 11 (Family: none)             | 1, 3-14  |
| Y  | JP, 7-111341, A (NEC Corp.),<br>25 April, 1995 (25. 04. 95),<br>Full text ; Figs. 1 to 6 & EP, 0653741, A1              | 1, 3-14  |
| Y  | JP, 60-202682, A (NEC Corp.),<br>14 October, 1985 (14. 10. 85),<br>Full text ; Figs. 1, 2 (Family: none)                | 4-7  |
| Y  | JP, 4-212287, A (Toppan Printing Co., Ltd.),<br>3 August, 1992 (03. 08. 92),<br>Full text ; Figs. 1 to 5 (Family: none) | 3-5, 8-9,<br>12-13   |
| <input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.  |   |  |
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| Date of the actual completion of the international search<br>9 November, 1998 (09. 11. 98)   |   | Date of mailing of the international search report<br>24 November, 1998 (24. 11. 98) |
| Name and mailing address of the ISA/<br>Japanese Patent Office   |   | Authorized officer   |
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